3D vertical resistive switching random-access memory (3D-VRRAM) for high density, high accuracy in-memory computing

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The rise of artificial intelligence imposes a heavy computational burden on traditional digital computing systems based on the von Neumann architecture. In-memory computing (IMC) is a non-von Neumann computing paradigm where highly specialized tasks are executed in parallel within memory arrays, thus benefiting the energy efficiency and the latency during data-intensive workloads. Resistive random-access memory (RRAM) appears as one of the most promising devices for IMC, featuring non-volatile multilevel storage, low-voltage/low-current operation, and scalability. A key enabler for RRAM technology is 3D vertical architectures [1], which allow a significant increase of the memory array density. This work addresses the recent progress of 3D-VRRAM structure and IMC results published in our previous work [2].

Fig. 1a illustrates a 3D-VRRAM cross-bar array (vCBA). The vCBA comprises vertically oriented Ti pillar top-electrodes (TEs) with a HfO_x switching layer deposited on the sidewalls by sputtering, and Pt planar bottom-electrodes (BEs) stacked with SiO_2 spacers. Fig. 1b shows the top view of a fabricated 3x3 vCBA. Fig. 1c shows a scanning electron microscope (SEM) image of the vertical hole sidewall after dry etching, where bright Pt layers are alternated with SiO_2 layers. Fig. 1d shows the switching I-V curves of the 3 cells on the same pillar TE, obtained by applying a voltage across the individual devices. The low-resistance state (LRS) shows relatively low variation as a function of cycles and layers, supporting the stability of the RRAM process. Multilevel cell (MLC) operation of the device was also demonstrated by gradual set or reset via program and verify algorithm [2]. Fig. 2a shows the representative matrix-vector-multiplication (MVM) circuit and methodology. After device programming, a voltage vector between -0.2 V and 0.2 V is applied to the TEs with grounded BEs, and the resulting current vector is measured at the output, satisfying the MVM operation $\vec{I} = G\vec{V}$. Fig. 2b shows the correlation plot between the experimental MVM results for vCBAs programmed in various target conductance matrices and the ideal results obtained with floating point 64-bit precision. Fig. 2c shows the circuit sketch for the inverse MVM operation, which expands the IMC concept to more linear algebra primitives [3]. The vCBA is connected in the feedback branch of operational amplifiers (OA), to solve a linear system according to $\vec{V} = -G^{-1}\vec{I}$. Fig. 2d shows an example of oscilloscope traces collected at the output of the OAs. The steady state voltage values correspond to the solution of a linear system.

In conclusion, 3D-VRRAM arrays show small cell size, controllable MLC programming and accurate algebra computing in both open-loop and closed-loop operation, thus supporting the strong potential of 3D-VRRAM technology for high density, energy efficient IMC.

References

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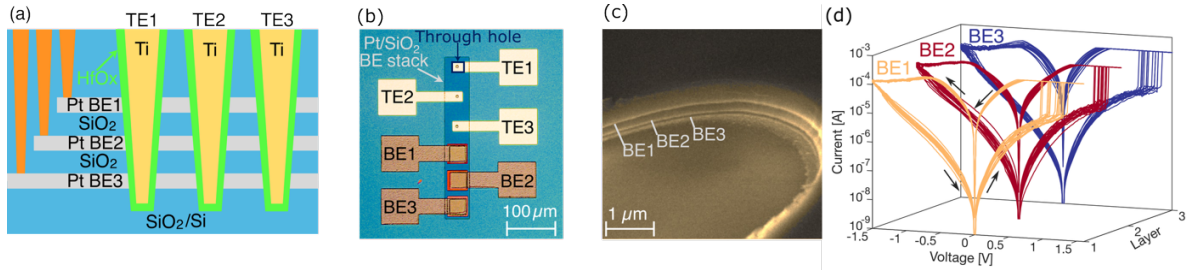

Figure 1 (a) Side-view sketch of 3D-V RRAM array. The Pt planar electrodes (grey) act as BEs and are separated by SiO_2 spacers (blue), and metal vias (orange) are realized to enable electrical probing. The pillar electrodes are realized with Ti (yellow) and HfO_x (green) is deposited on the sidewall as active switching oxide. (b) Top-view of a fabricated 3x3 vCBA. (c) SEM image of the hole sidewall after dry etching. (d) Set/reset I-V curves for each layer.

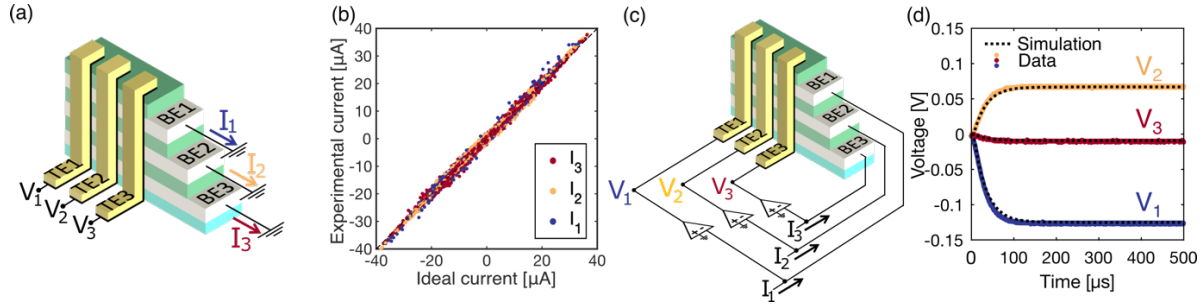

Figure 2 (a) Sketch of the MVM configuration. Voltages between -0.2 V and 0.2 V are applied to the TEs with grounded BEs, and the resulting measured currents correspond to the result of the operation: $\vec{I} = G\vec{V}$. (b) Correlation plot between experimental MVM values and ideal ones calculated with floating-point precision on the weights. (c) Closed-loop IMC circuit in which the vCBA is connected in the feedback branch of OAs acting as gain stage. The relation between the input currents and output voltages is given by: $\vec{V} = -G^{-1}\vec{I}$. (d) Example of measured voltages traces at the output of the OAs compared with the SPICE simulation of the closed-loop circuit.